

FIG. 1

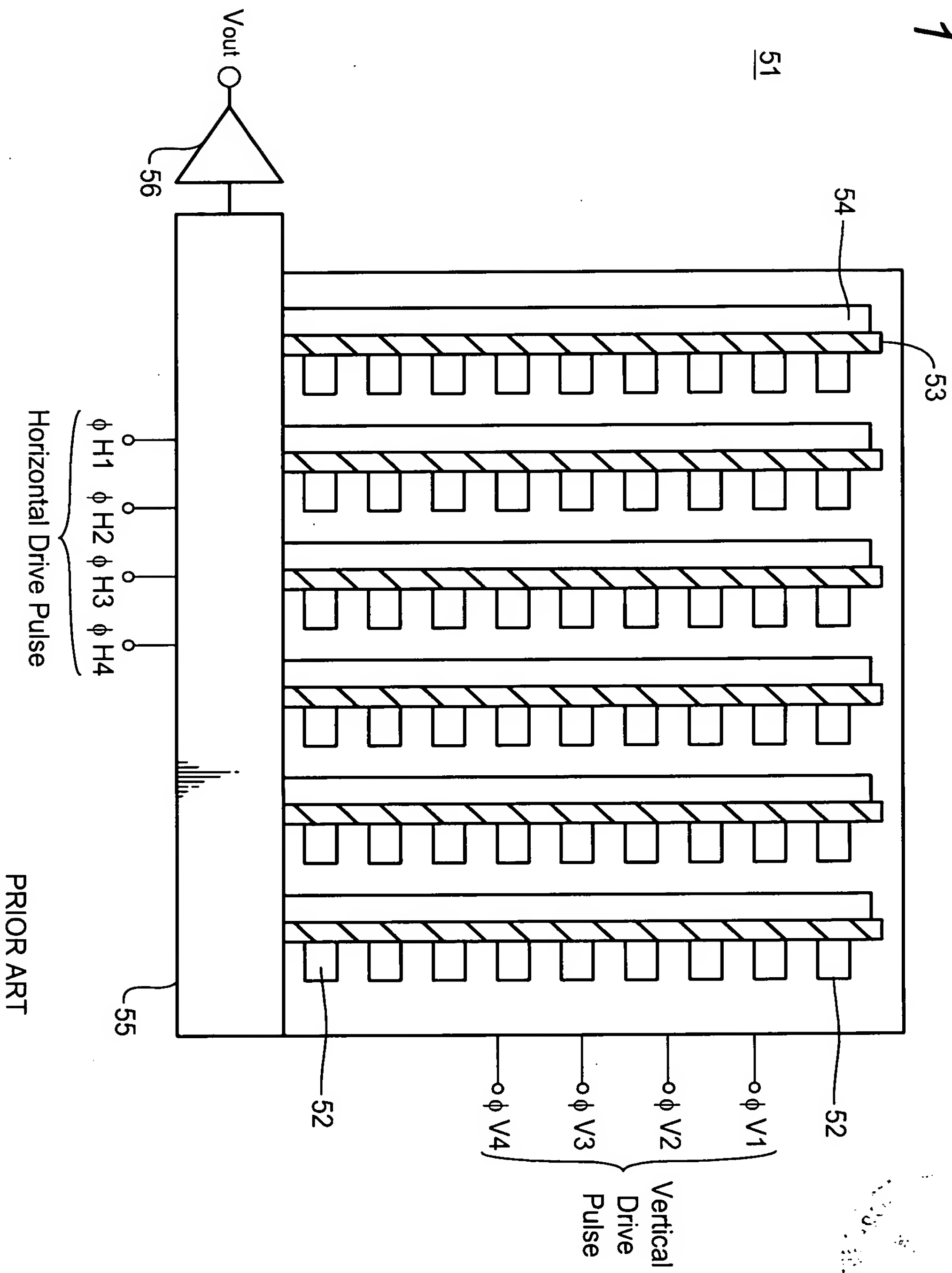
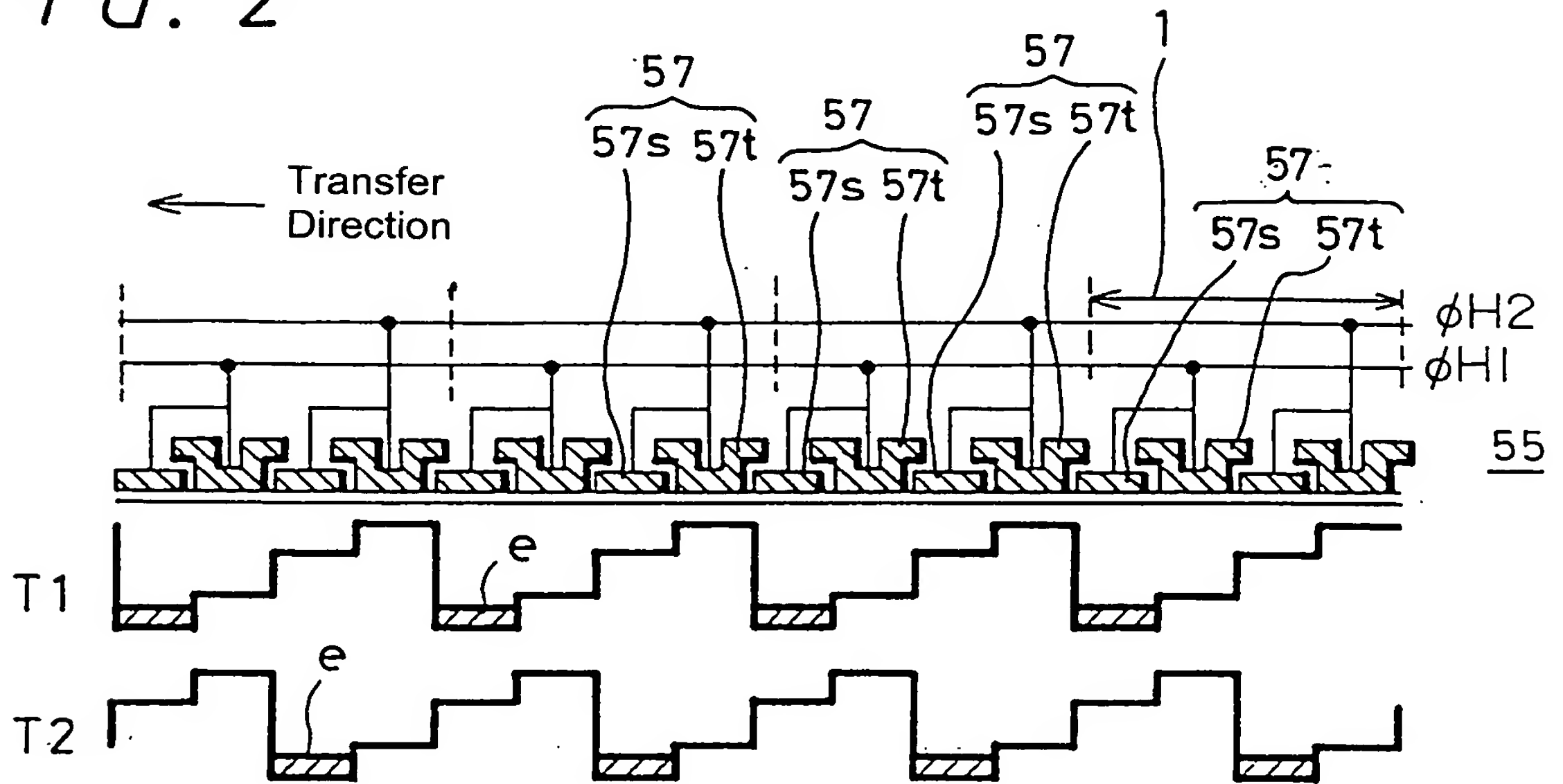
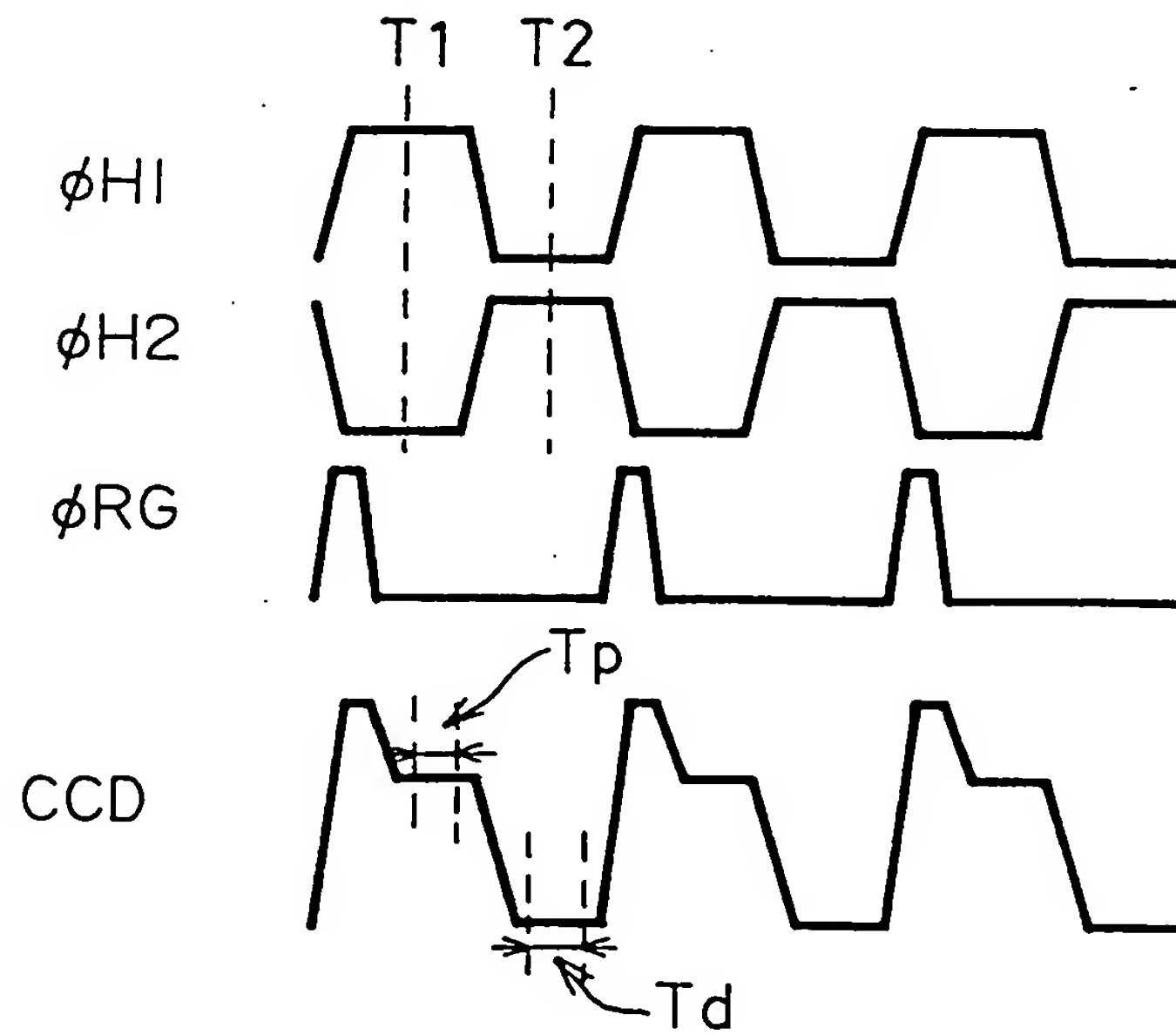


FIG. 2



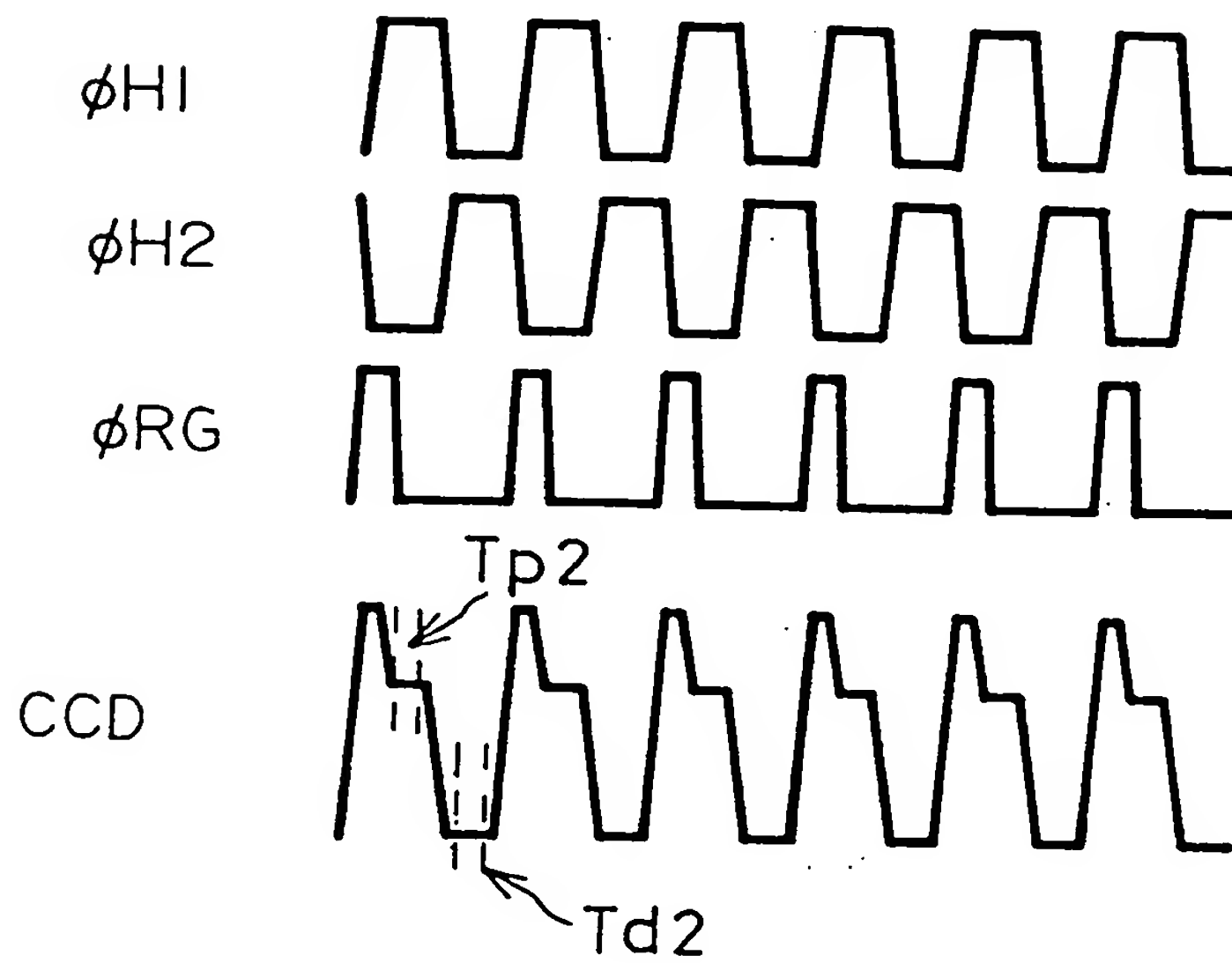
Prior Art

FIG. 3



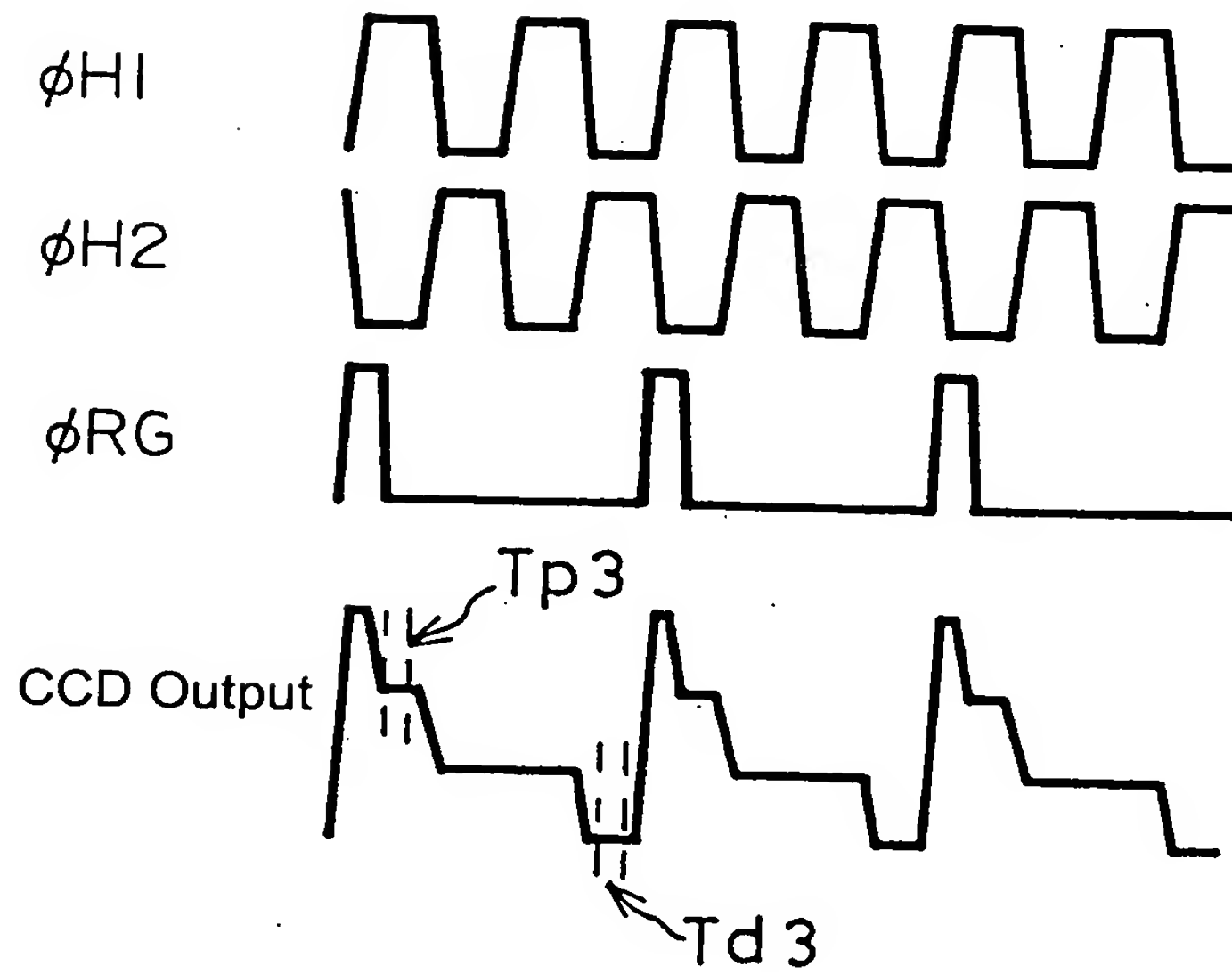
Prior Art

FIG. 4



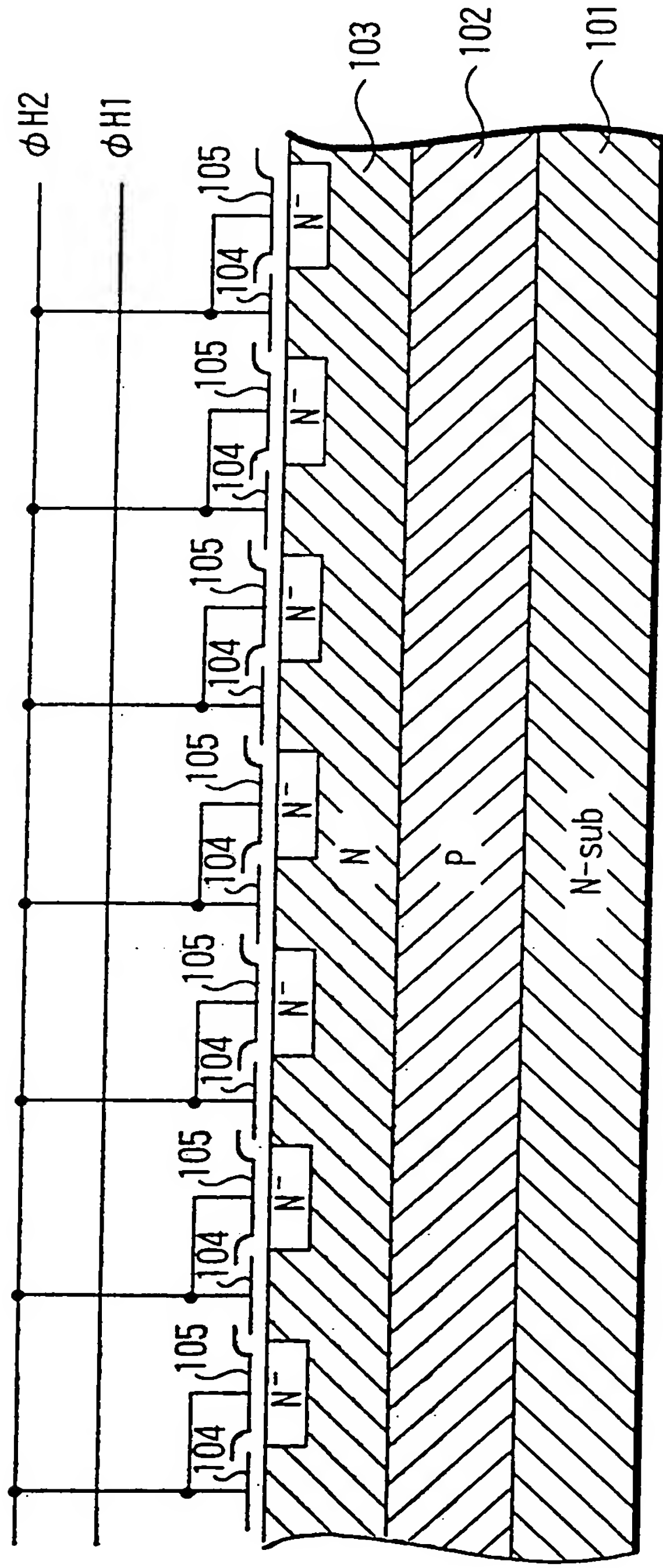
Prior Art

FIG. 5



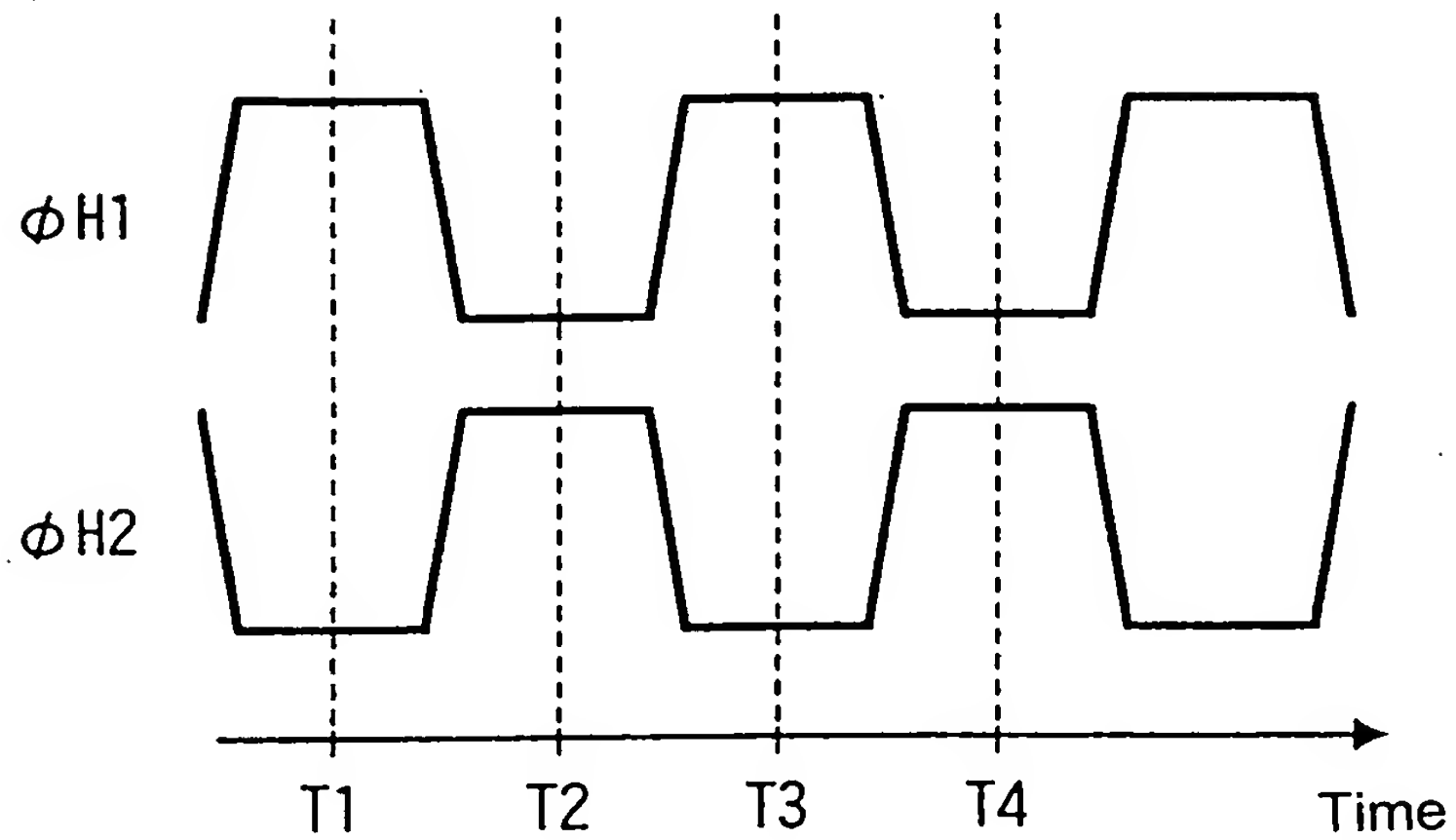
Prior Art

FIG. 6

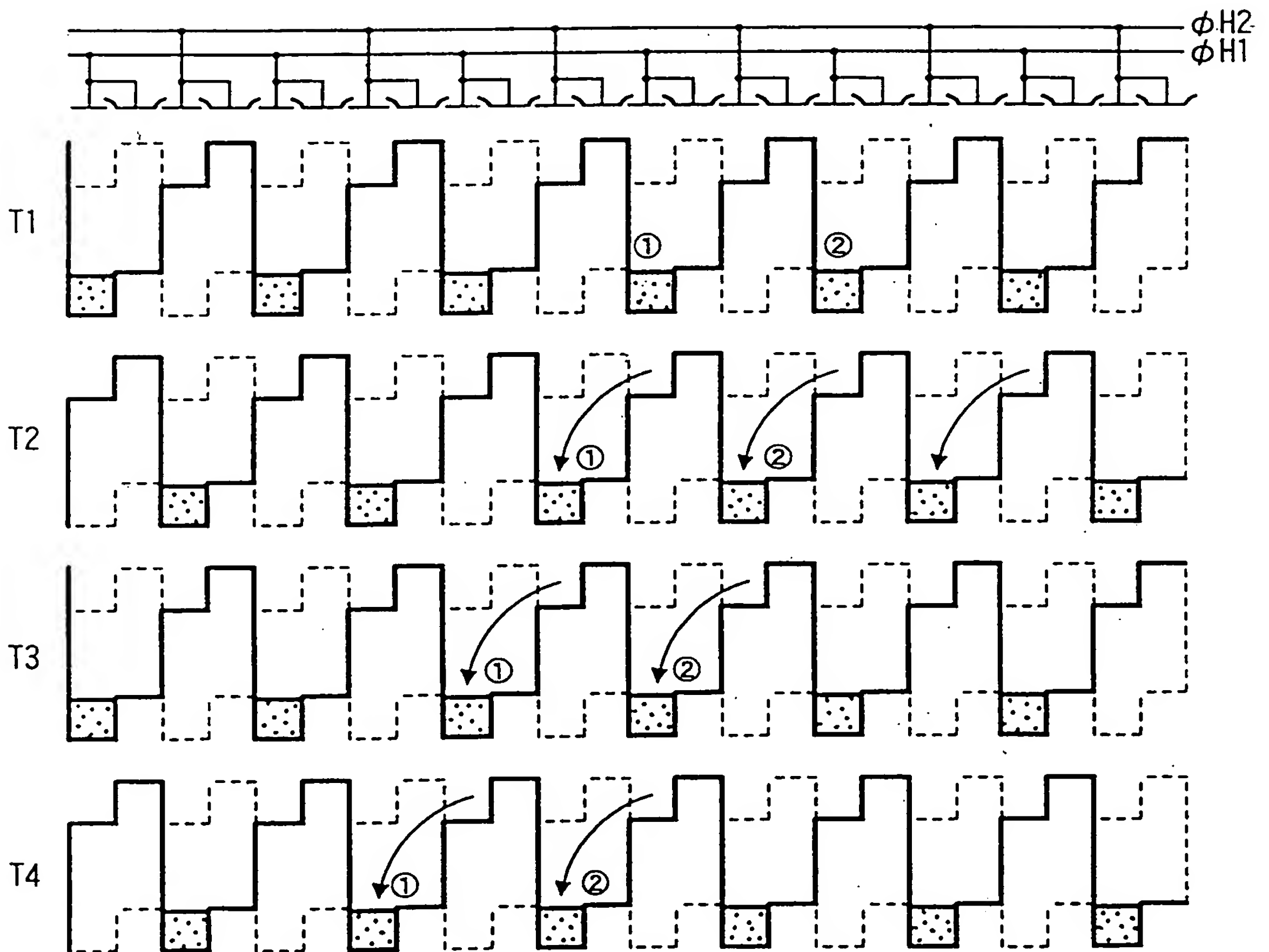


Prior Art

*F / G. 8*



## Prior Art



## Prior Art

FIG. 9

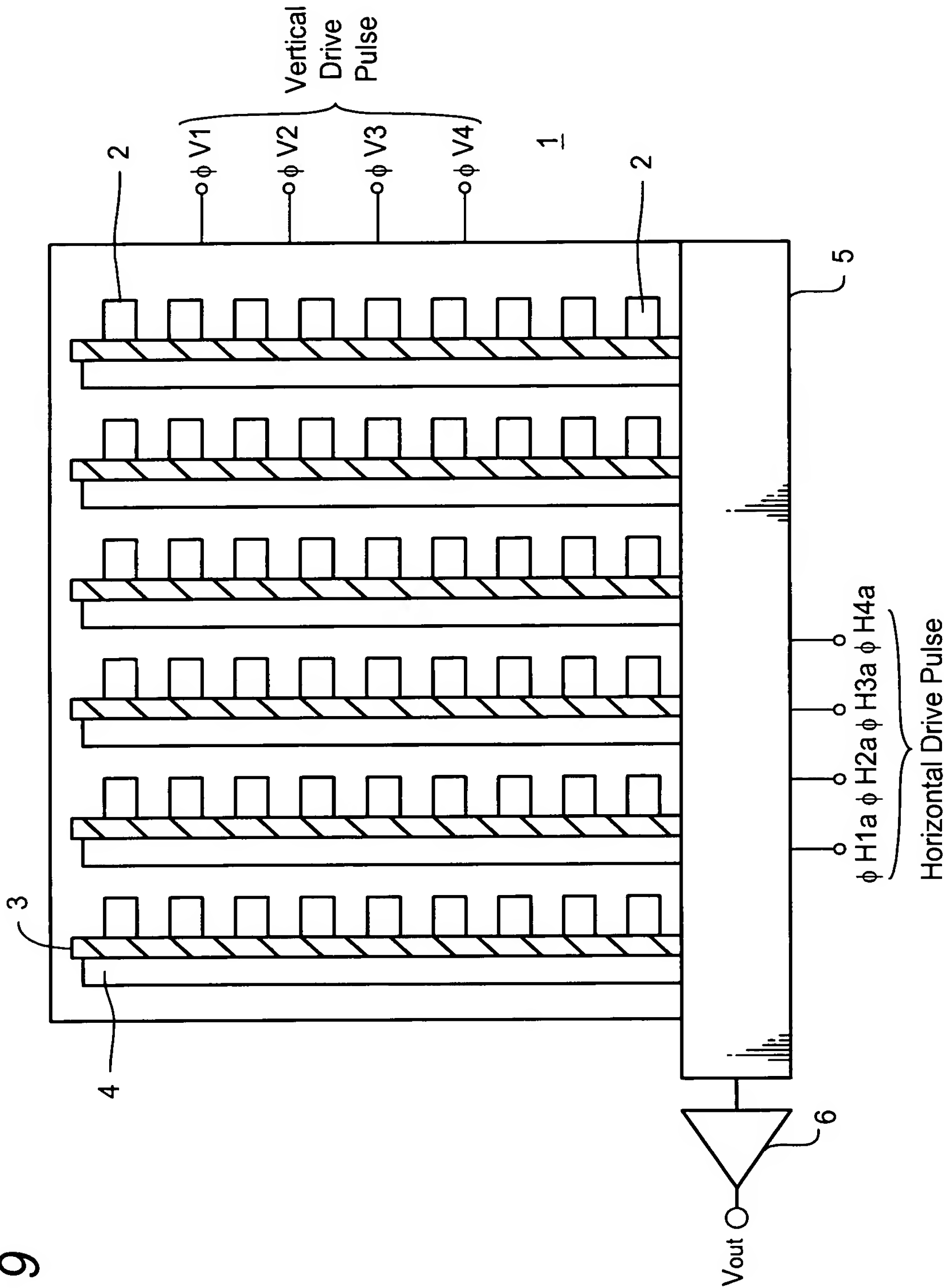


FIG. 10

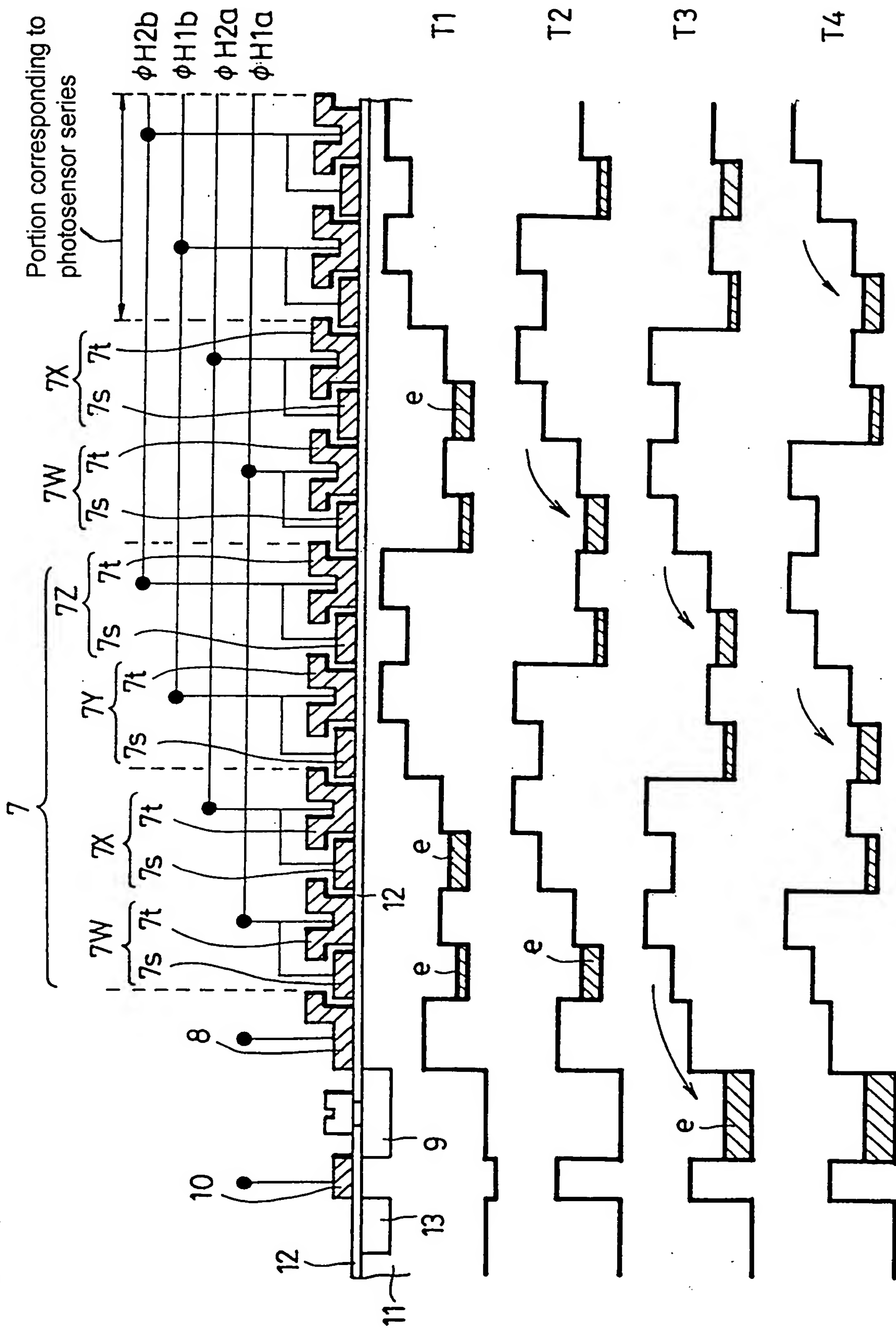


FIG. 11

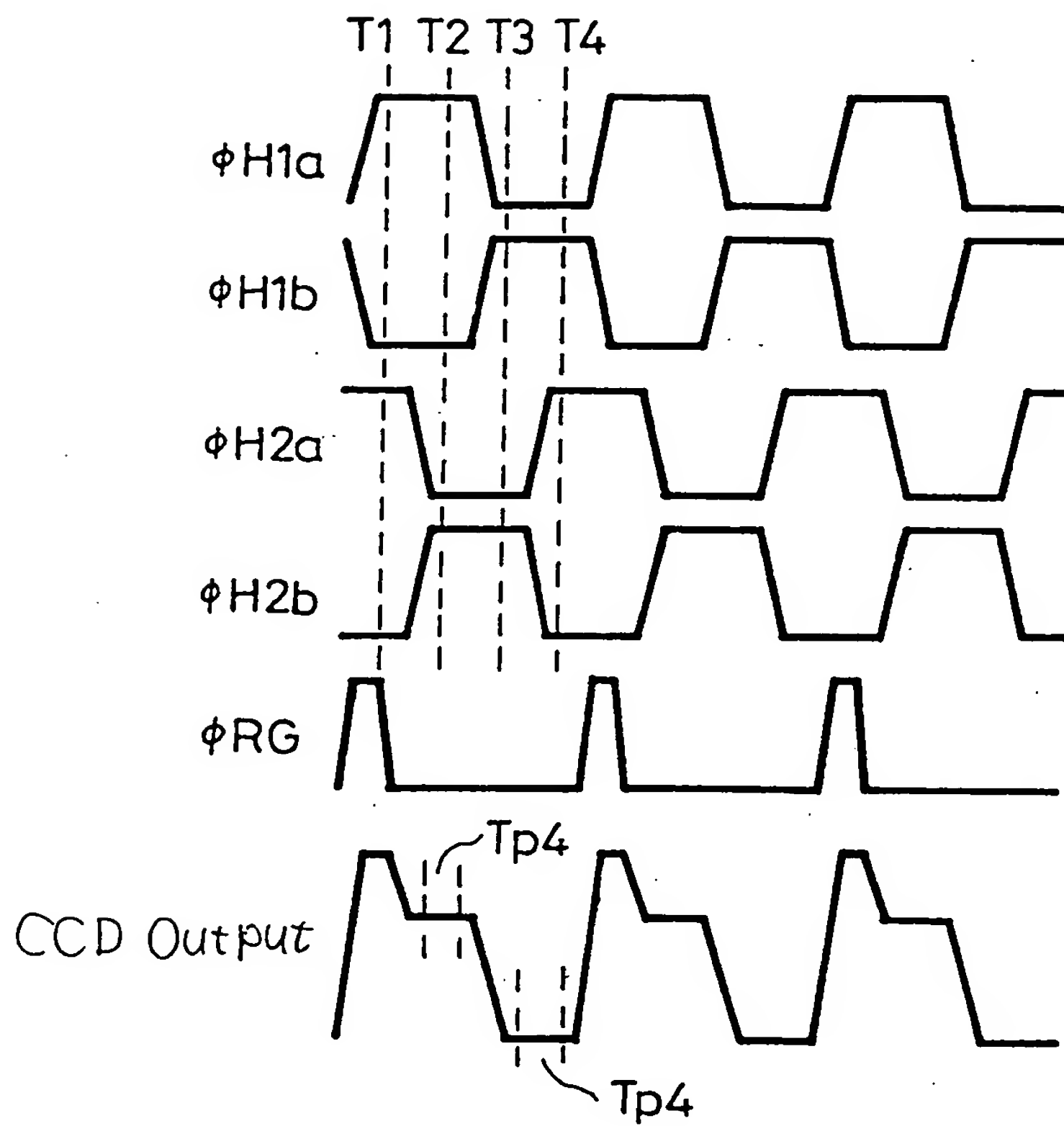




FIG. 12A

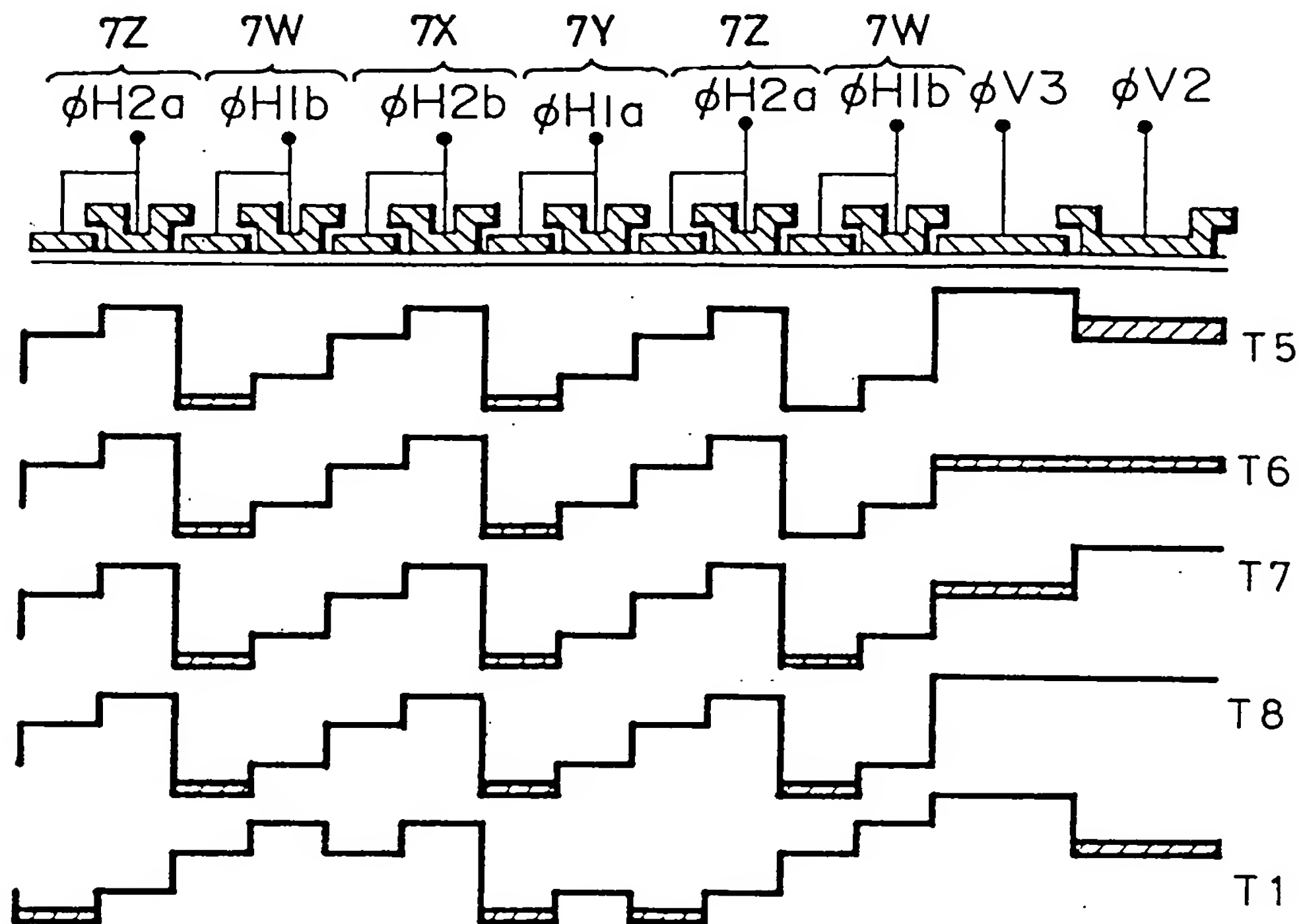


FIG. 12B

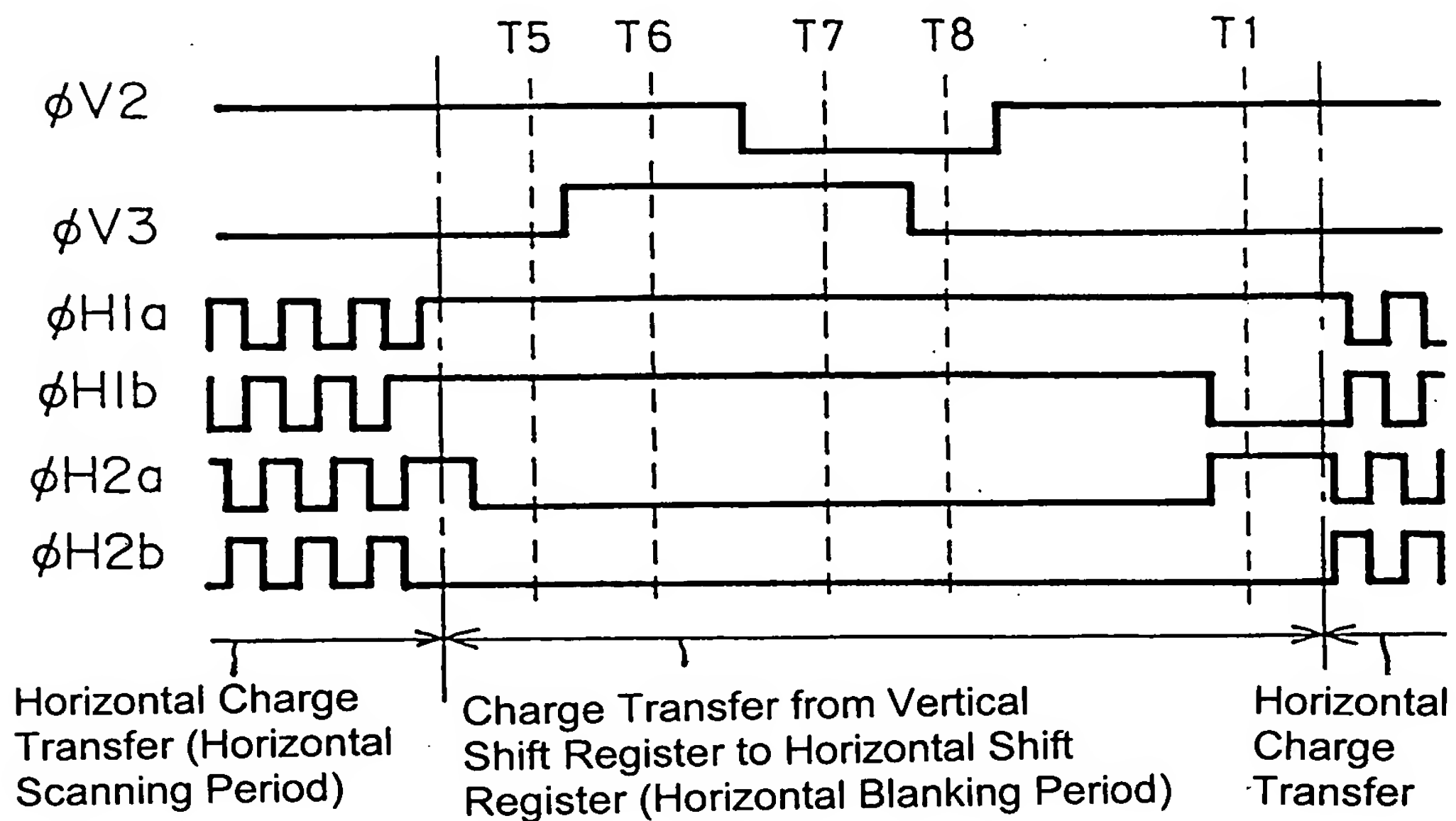


FIG. 13

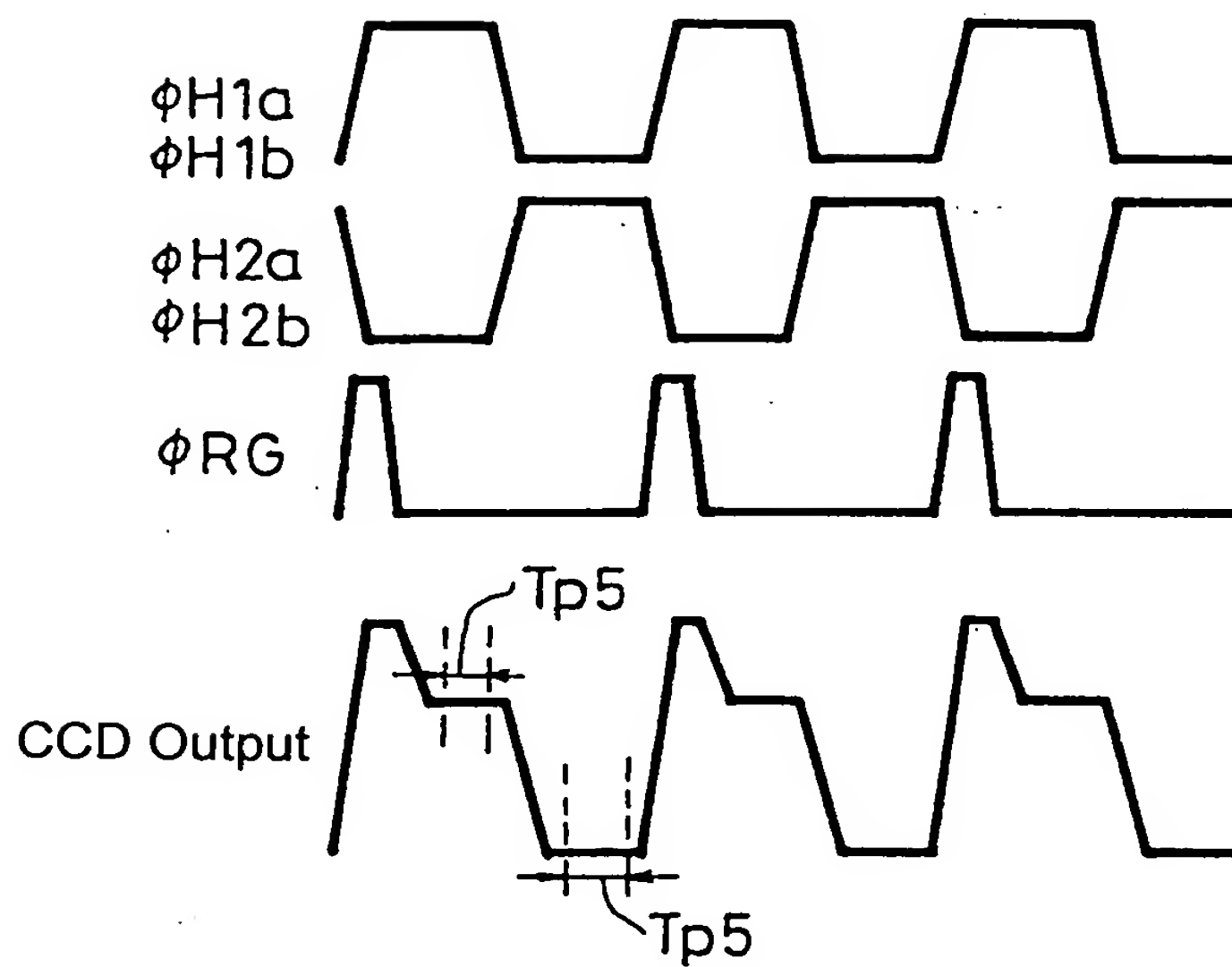
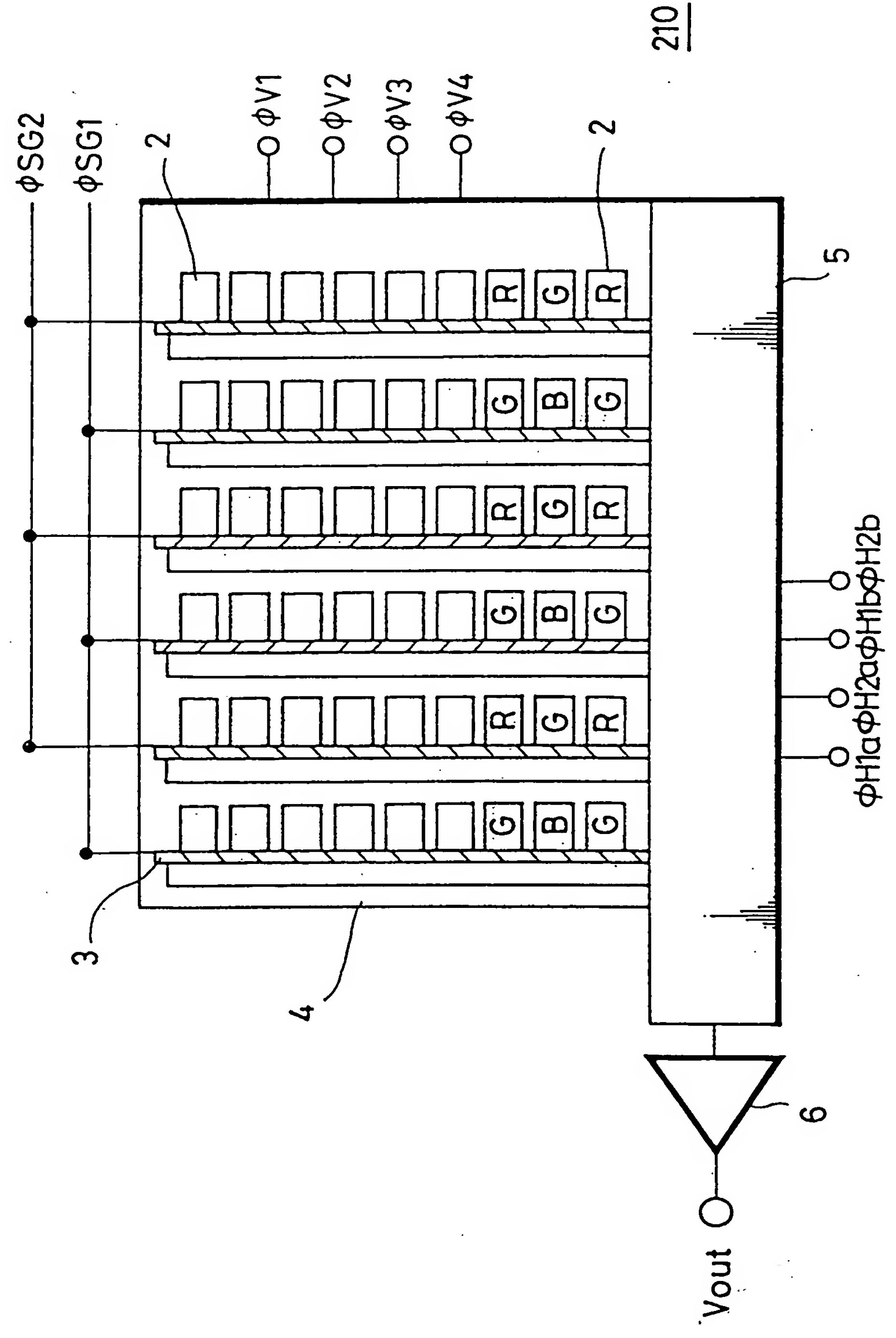


FIG. 14



210

FIG. 15

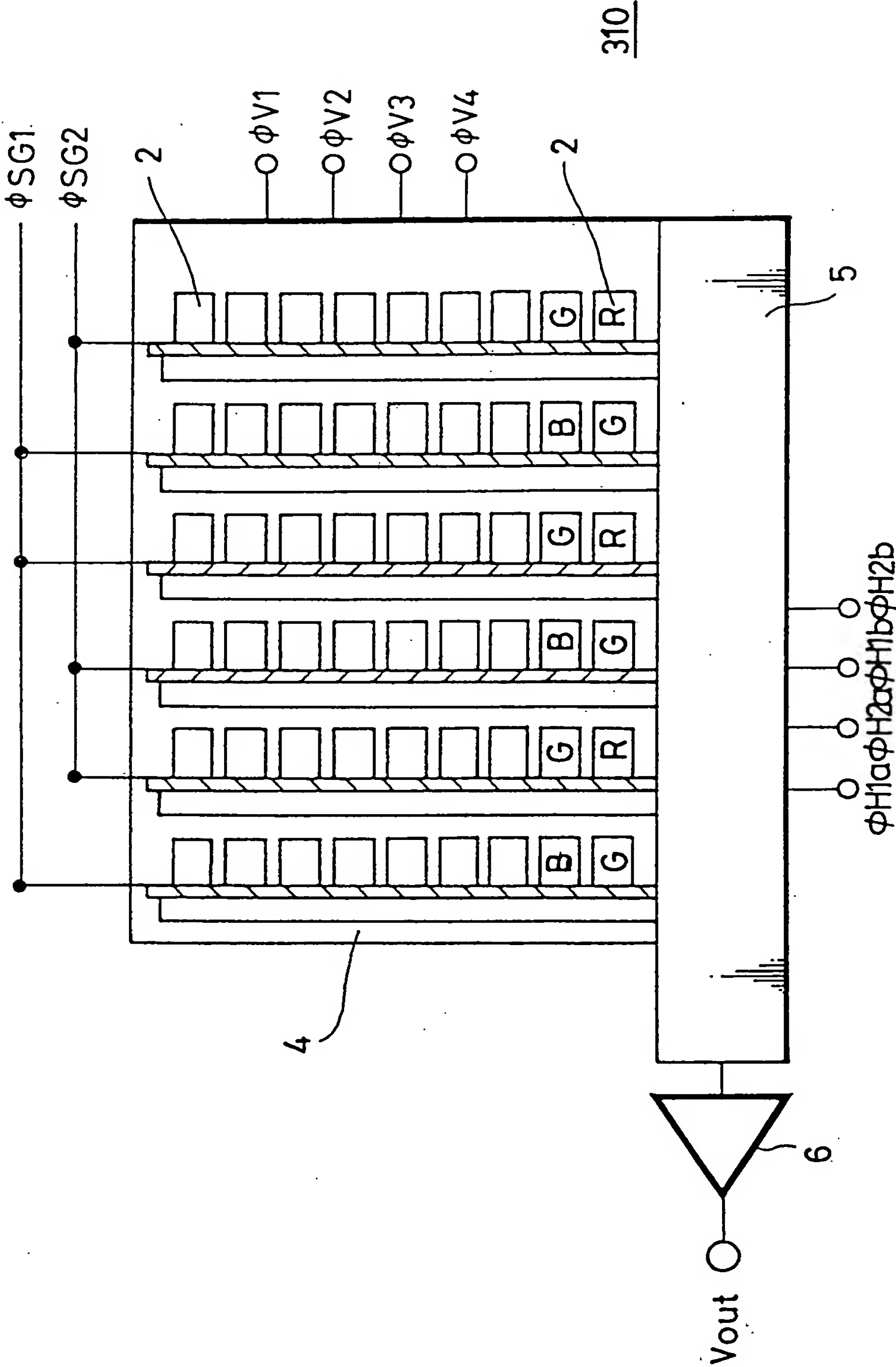


FIG. 16

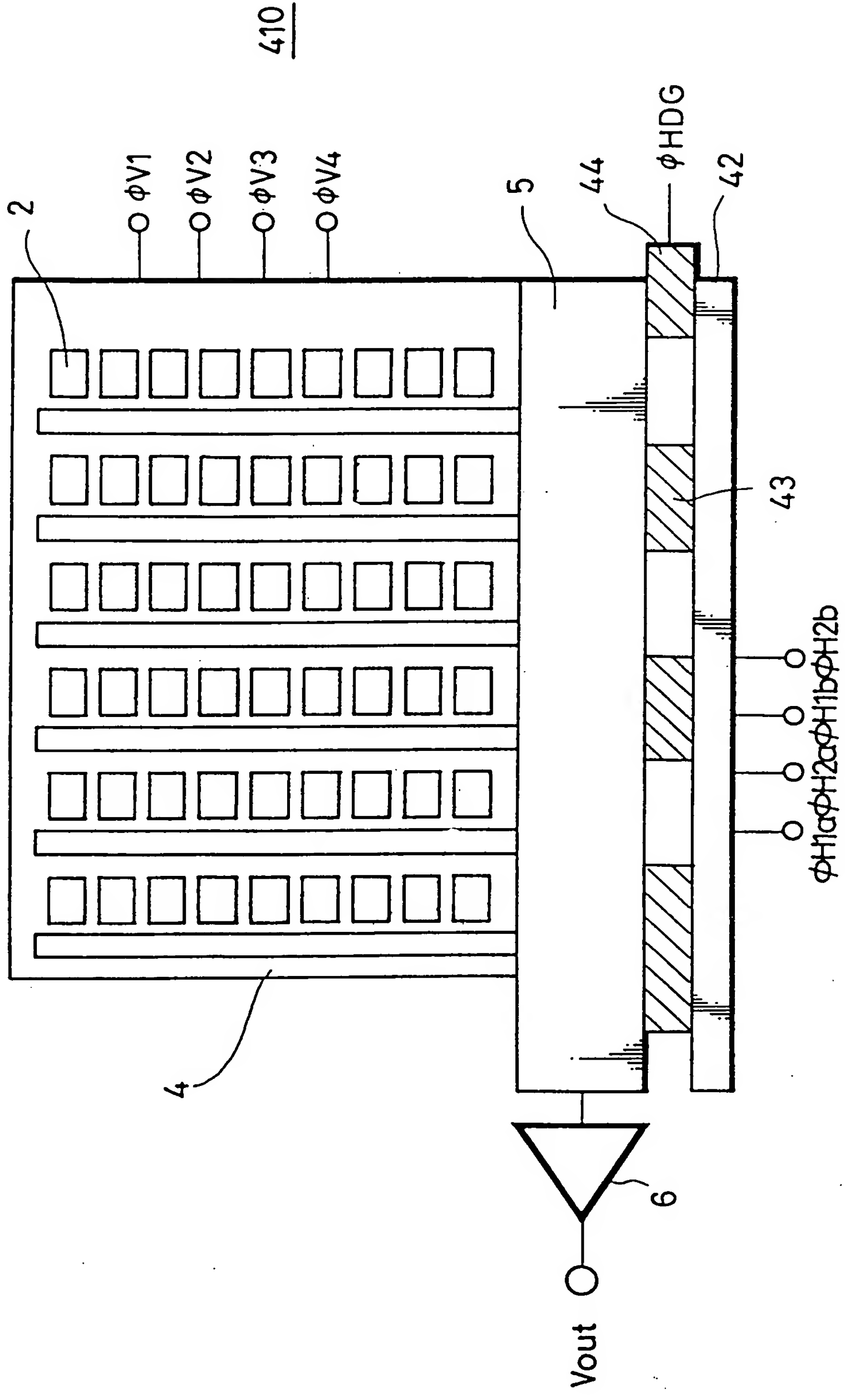
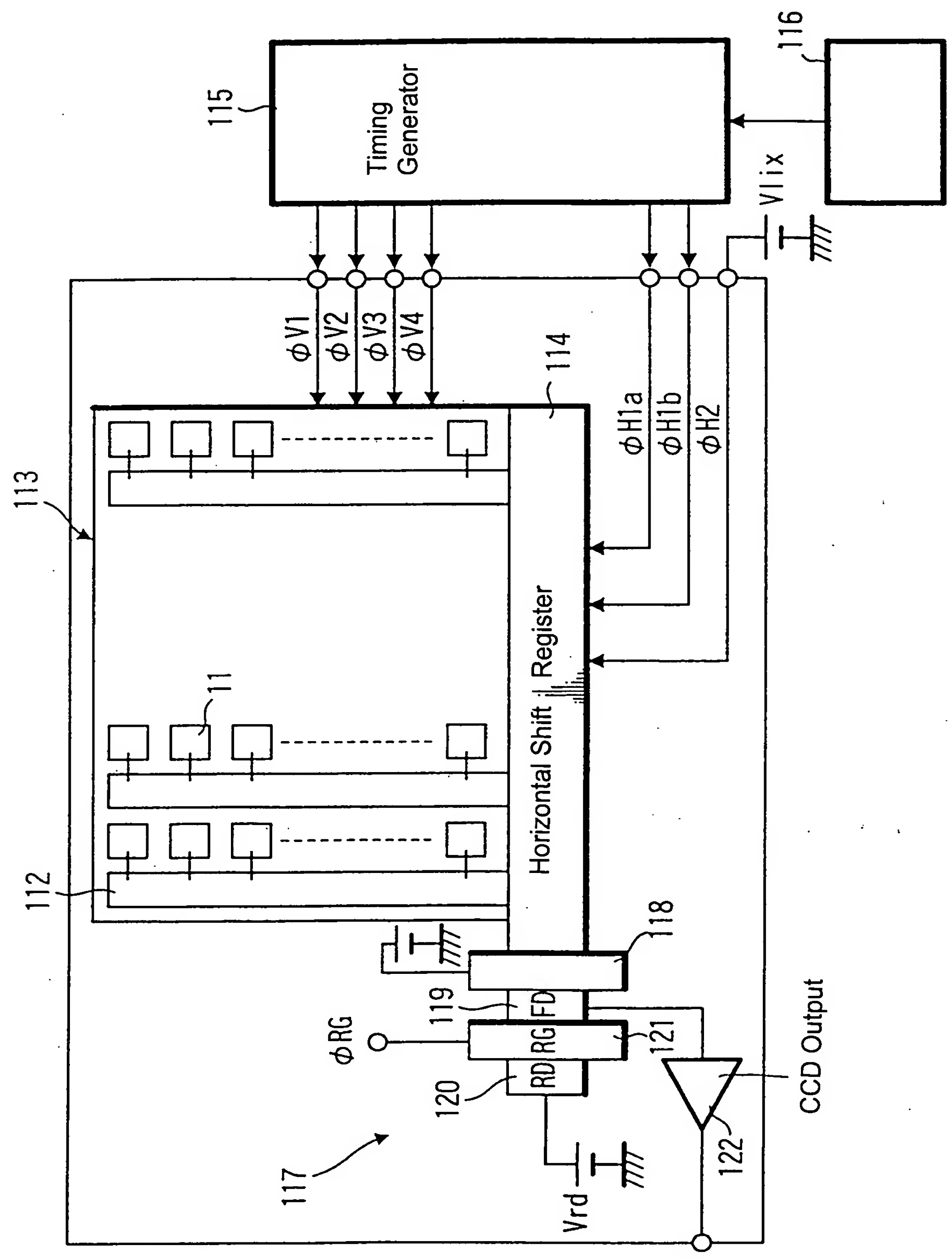
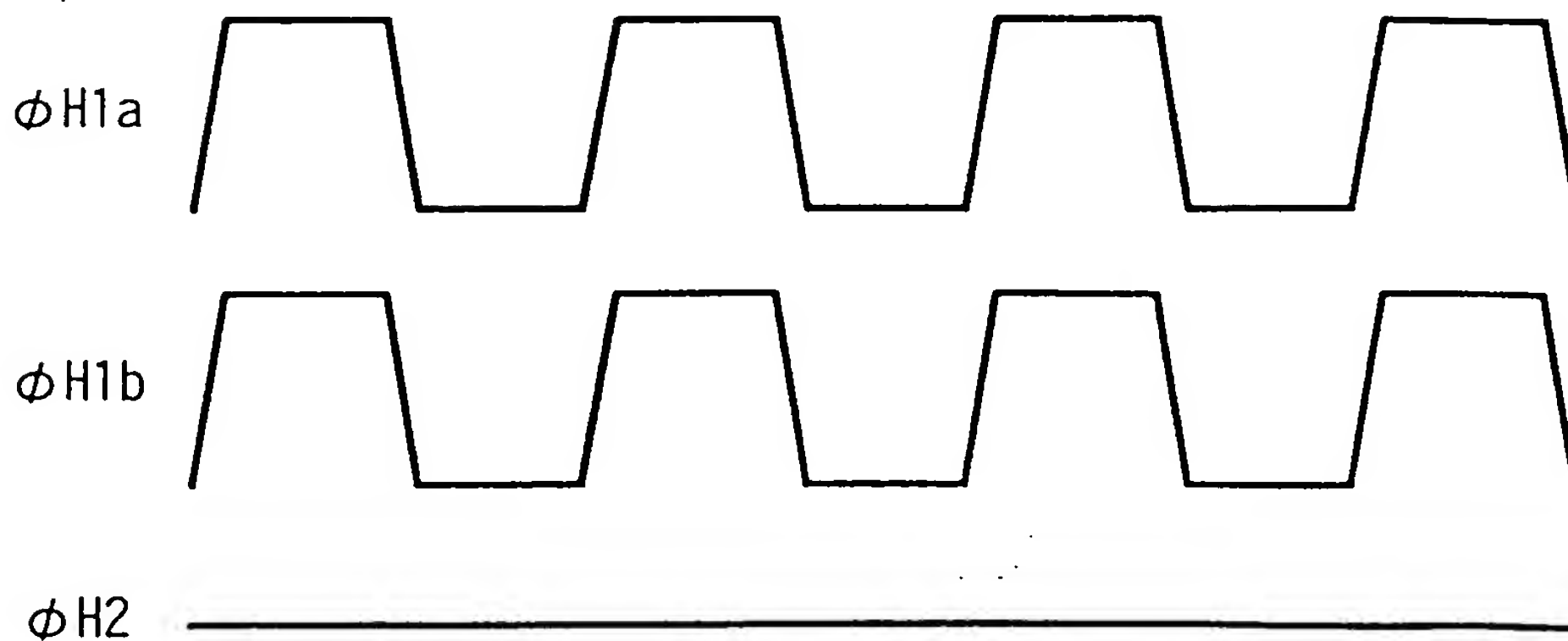


FIG. 17



*FIG. 18A*



*FIG. 18B*

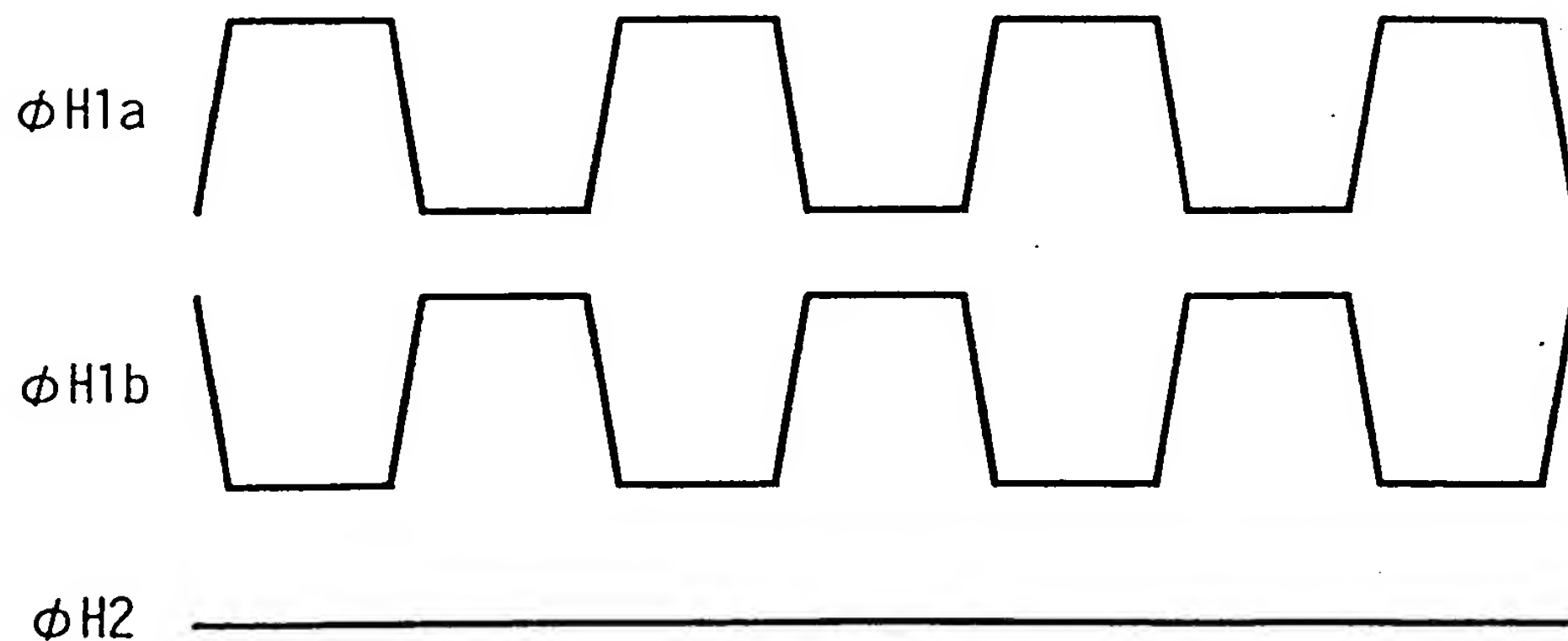


FIG. 19

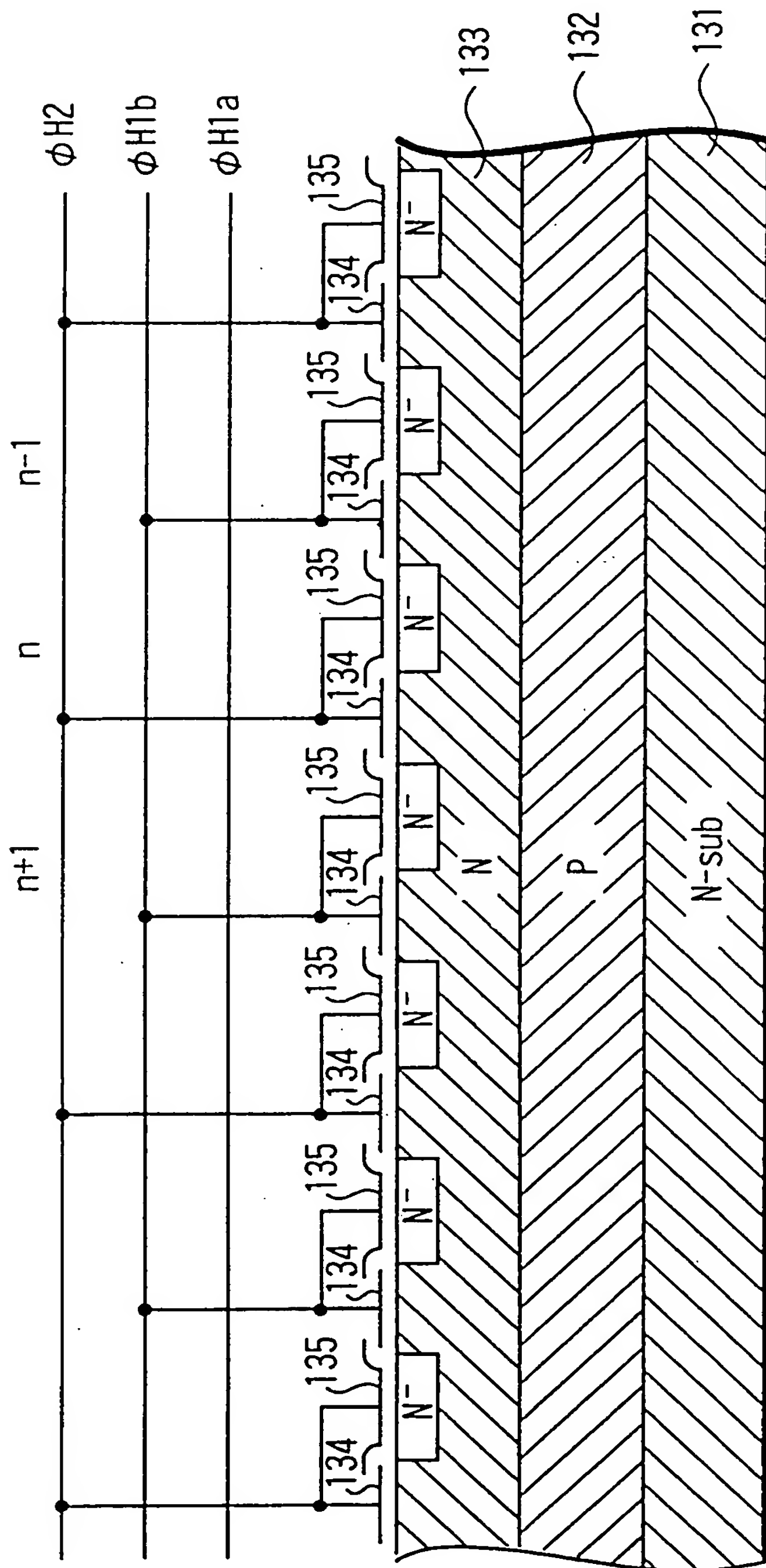




FIG. 20A

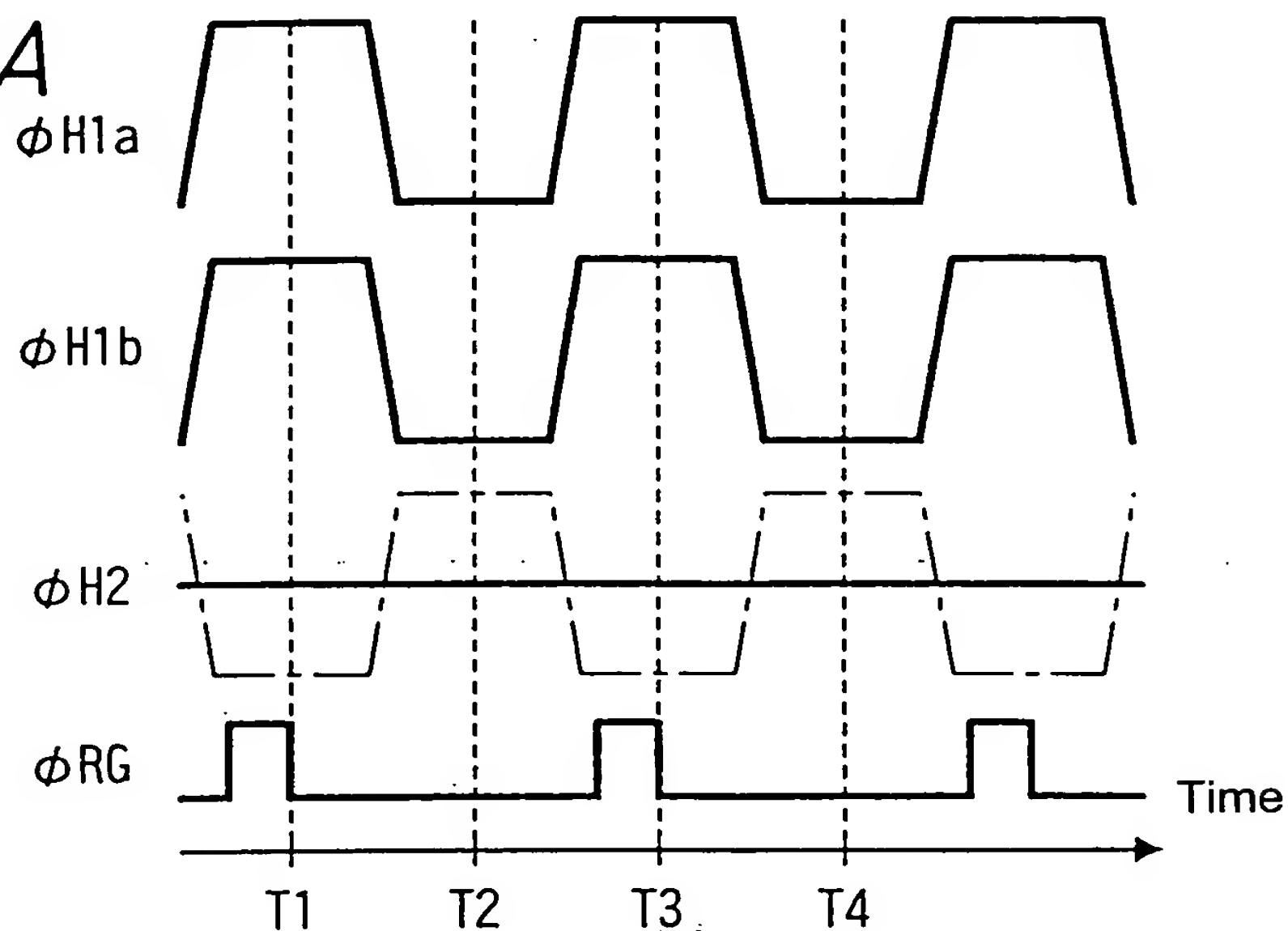


FIG. 20B

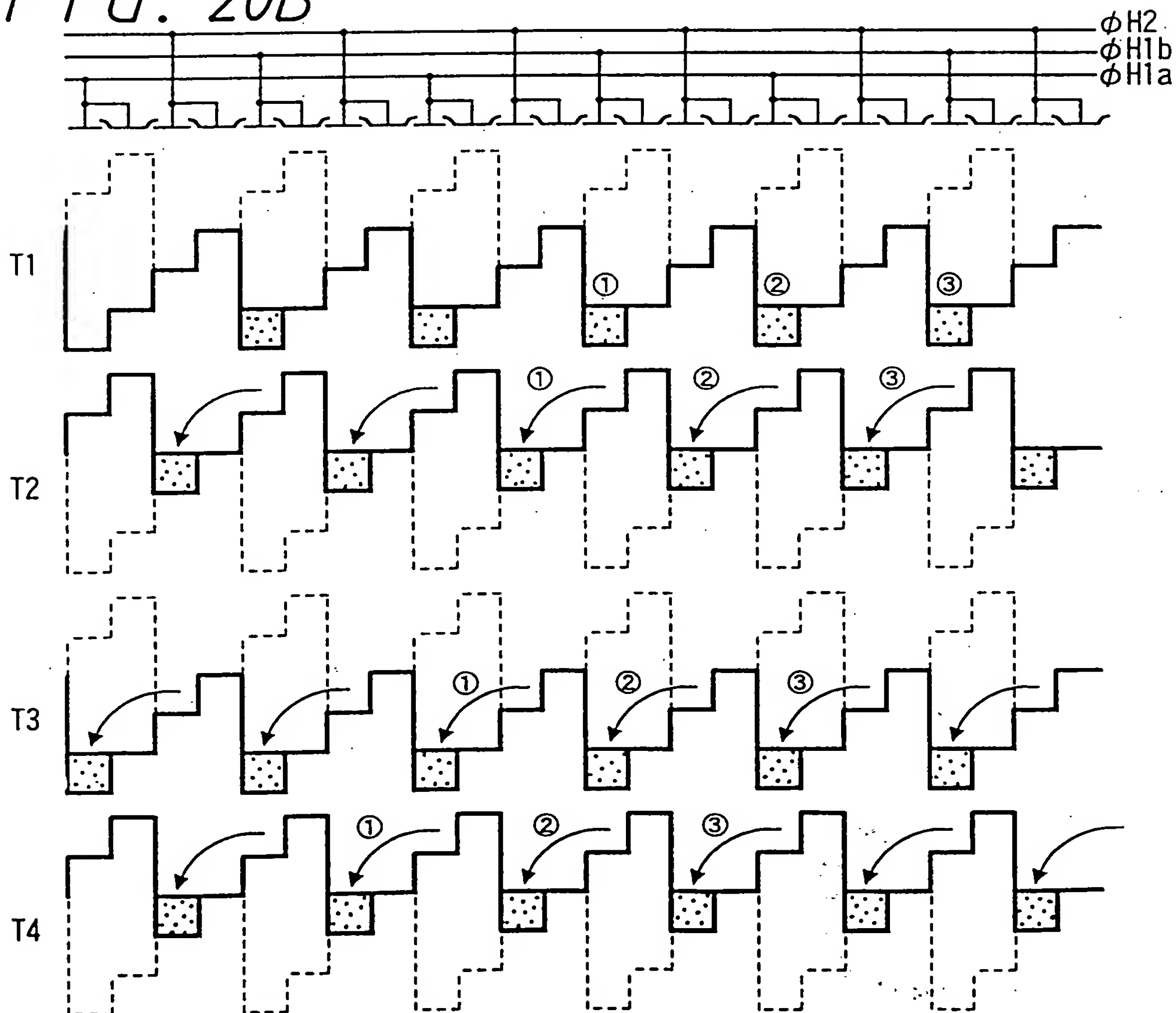


FIG. 21A

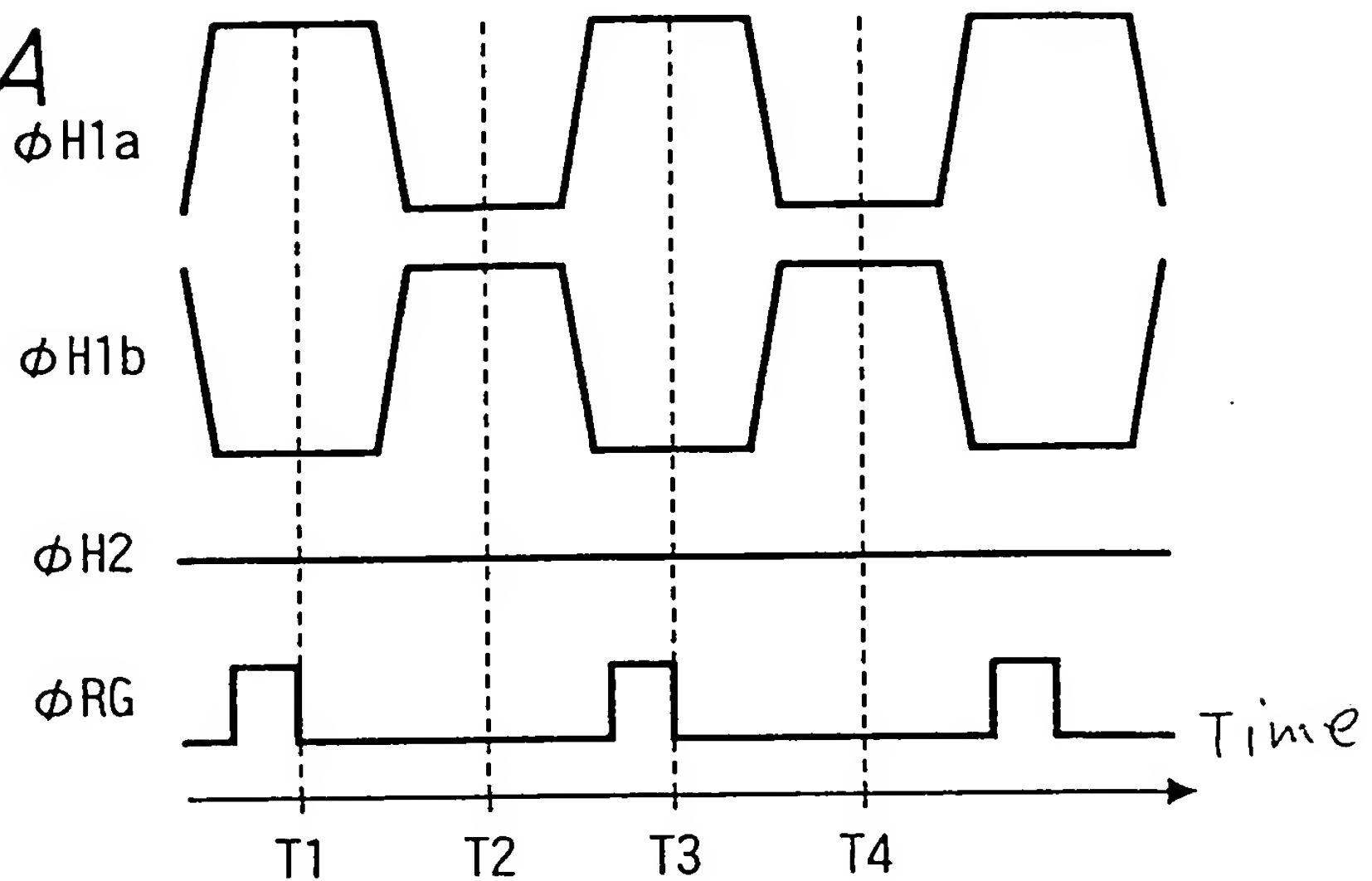


FIG. 21B

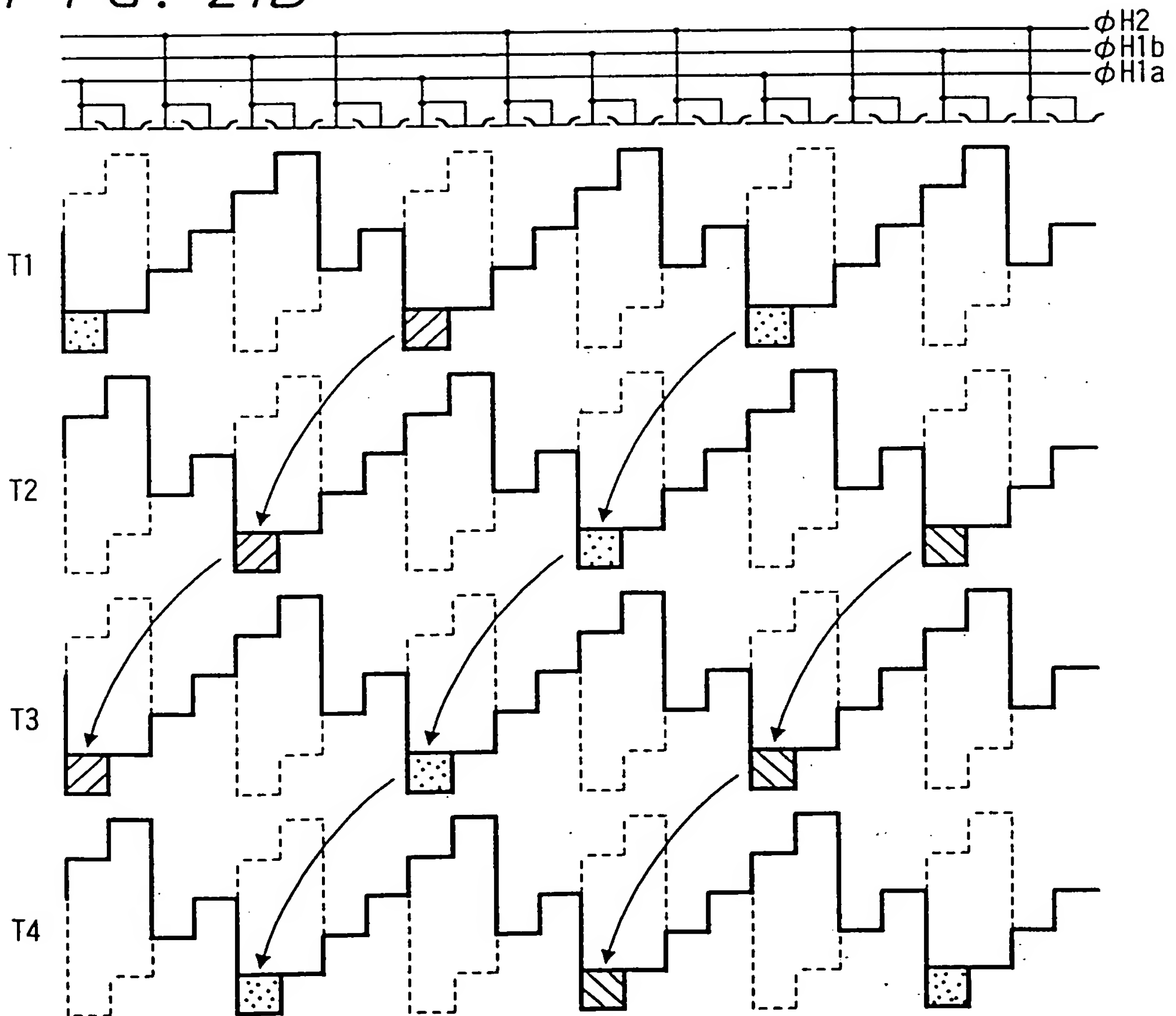
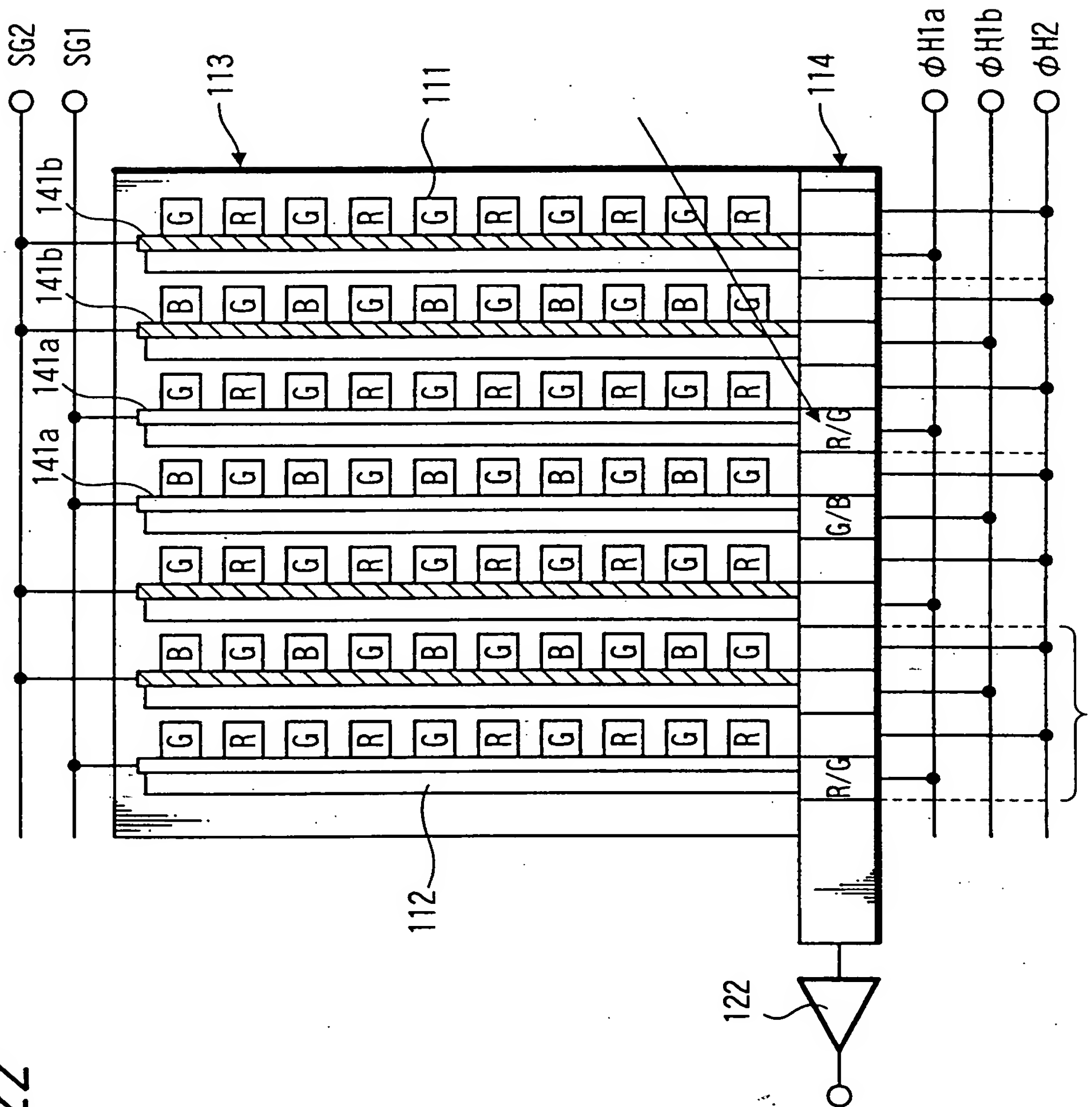


FIG. 22



**FIG. 23**

The diagram illustrates a CCD array structure. The array is organized into a grid of color filters (G, R, B) and is divided into four horizontal sections (148) and four vertical sections (146). The readout circuit includes a vertical shift register (112) and a horizontal shift register (114). The output of the horizontal shift register is connected to a CCD output (122). The readout circuit is controlled by clock signals  $\phi H1a$ ,  $\phi H1b$ , and  $\phi H2$ . A portion of the array is labeled "Portion where signal changes are transferred from vertical shift register to horizontal shift register (Odd/Even line)".

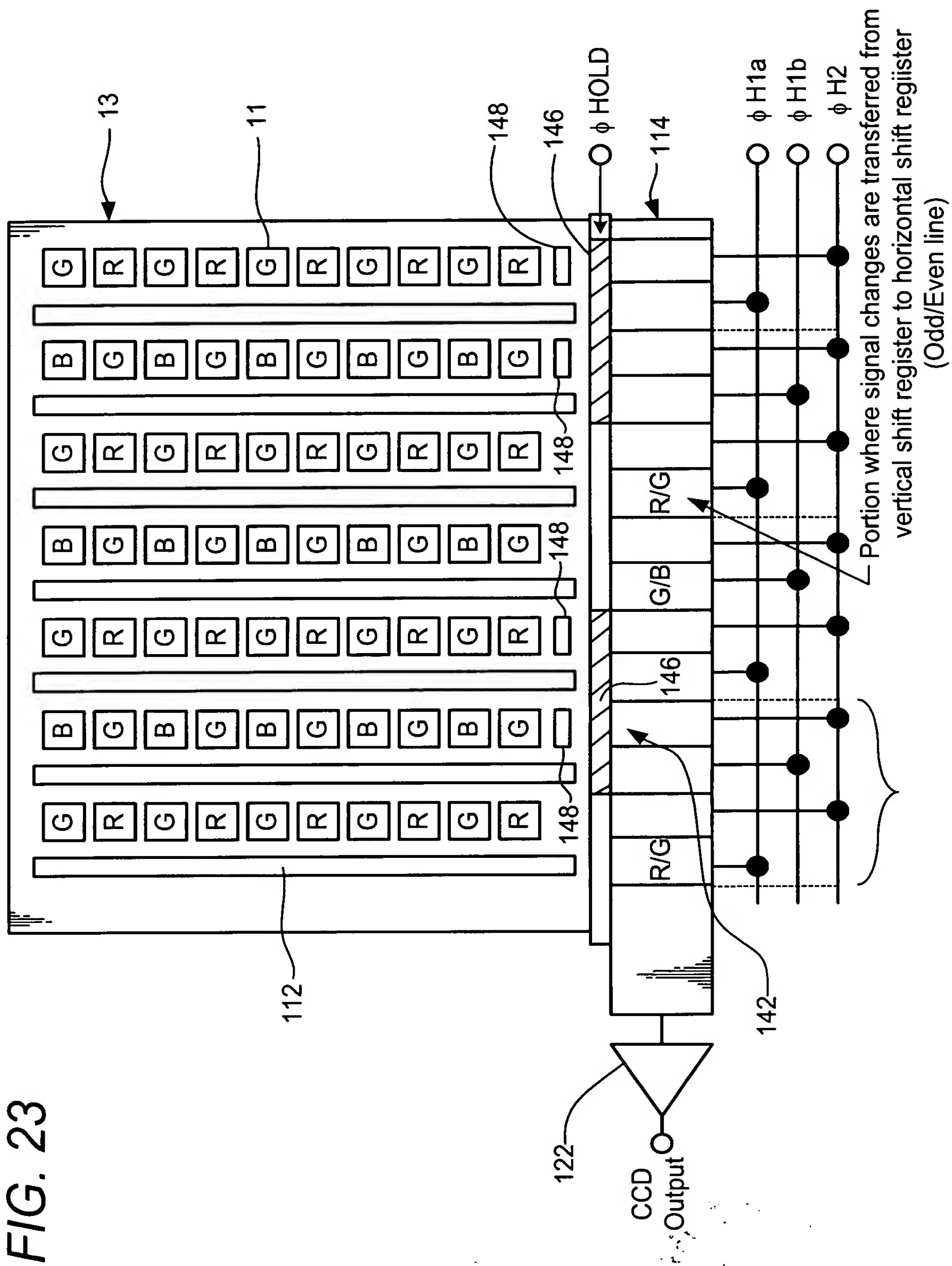


FIG. 24

